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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,979	07/28/2003	Hieu Van Tran	2102397-991400	7148

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EXAMINER	
NGUYEN, VIET Q	
ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 04/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SM

Office Action Summary	Application No.	Applicant(s)	
	10/628,979	TRAN ET AL.	
	Examiner	Art Unit	
	Viet Q. Nguyen	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Election filed on 2/17/2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-97* is/are pending in the application.

4a) Of the above claim(s) *54-97* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6-9,15-20 and 27* is/are rejected.

7)☒ Claim(s) *2-5,10-14,21-26 and 28-53* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The applicant's election of Group **1**, claims **1-53**, with traverse is acknowledged.

In response to applicant's remarks, the different groups belong to different classes and/or different claimed subject matter that certainly require lot of examiner's attention and careful hours of both searching and examination in order to be complete and thorough work for each of these claimed technology areas or subject matters Furthermore, with the fast growing of the issued patents of today, more time is necessary for the examiner to search and study each patent so to ensure a very quality issued patent/product. If all of these groups are joined together in a single examination process, that would probably reduce the quality of examination. Thus, the rejection is final and other claims **54-97** are withdrawn from further consideration.

Claims **1-53** are present for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims **1, 6-9, 15-16, 27** rejected under 35 U.S.C. 103(a) as being unpatentable over **Miller et al (4,885,720).**

Miller (see Fig.1A) clearly shows a memory device having a first, normal memory array (100) and a second, redundant memory array (102), a plurality of main wordline drivers (140) acting as the claimed "first y-drivers" and a main word line decoder (120) acting as the claimed first circuit for testing a level of stored data in the memory array (100), a plurality of redundant wordline drivers (142) acting as the claimed "redundant y-drivers" and an additional, redundant word decoder (122) for acting as claimed "second circuit for testing a level of stored data in the redundant array (102)". Note that col. 5 (lines 45-68) mentions that the memory testing for defective address is programmed into a redundant word decoder (using laser-blown fuses, etc.) and word line decoder performs the address switching. Thus, from this statement, one skilled in the art can see that testing & automatic replacement for all the stored, defective data the two arrays (100, 102) is obviously performed by these two claimed "first" and "second" circuits as well. Fig. 1A also shows the use of a main word line decoder and redundant word lien decoders for comparing the addresses on bus (150) with the stored defective address, and col. 6 (lines 9-11) further stated that "...***special provisions must be made such <u>that only one</u> of the main memory array (100) and the redundant array (102) is activated at a particular time***...", which obviously further suggests that only one array is enabled at a time and the other would be disabled. In order to accomplish this, Fig.1A further shows the use of selection circuit (130, 132) for selectively activate the corresponding y-drivers (140, 142) depending ion the compared address coming from the bus (150). Thus, it would be obvious that both circuits (130, 132) together acting as the claimed "controller" for generating a selection signal to

enable the redundant drivers (142) and to disable the main drivers (140) in response to the failure of testing by the main word decoder or corresponding first circuit (120) as recited.

Regarding claim **6-9, 15-16, 27**, the use of NAND gates and programmed fuses for comparing the address input pattern is shown in blocks (220, 222) and for enabling/disabling the particular decoders are shown.

3. Claims **1** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Lee et al (5,774,396).**

Lee et al (see Fig.1) clearly shows a memory device having a first, normal memory array (12) and a second, redundant memory array (shown as separate block 34). Fig. 3 shows a plurality of main wordline drivers (100) acting as the claimed "first y-drivers" and a main word line decoder (14, Fig. 1) also acting as the claimed first circuit for testing a level of stored data in the memory array (12), a plurality of redundant wordline drivers (130, see Fig. 3) acting as the claimed "redundant y-drivers" and an additional, redundant word decoder (32) for acting as claimed "second circuit for testing a level of stored data in the redundant array (102)". Note that col. 5 (lines 45-68) mentions that the memory testing for defective address is programmed into a redundant word decoder (using laser-blown fuses, etc.) and word line decoder performs the address switching. Thus, from this statement, one skilled in the art can see that testing & automatic replacement for all the stored, defective data the two arrays (100, 102) is obviously performed by these two claimed "first" and "second" circuits as well. Fig. 1A

also shows the use of a main word line decoder and redundant word lien decoders for comparing the addresses on bus (150) with the stored defective address, and col. 6 (lines 9-11) further stated that "...***special provisions must be made such that only one of the main memory array (100) and the redundant array (102) is activated at a particular time***...", which obviously further suggests that only one array is enabled at a time and the other would be disabled. In order to accomplish this, Fig.1A further shows the use of selection circuit (130, 132) for selectively activate the corresponding y-drivers (140, 142) depending ion the compared address coming from the bus (150). Thus, it would be obvious that both circuits (130, 132) together acting as the claimed "controller" for generating a selection signal to enable the redundant drivers (142) and to disable the main drivers (140) in response to the failure of testing by the main word decoder or corresponding first circuit (120) as recited.

3. Claims **1, 15, 17-20, and 27** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Tran et al (6,002,620).**

Tran et al (see Fig. 1A) clearly shows a memory device having a first, normal memory array (see 200 column drivers from COLDRV0 to COLDRV199) and a second, redundant memory array (shown as column drivers COLDRVR0 to COLDRVR1). Fig. 1A also shows a plurality of main wordline drivers (COLDRV0-COLDRV199) acting as the claimed "first y-drivers" and a main decoders (XDEC, CMDEC) also acting as the claimed first circuit for testing a level of stored data in the memory array with the help of the column MUX counter (CMCTR). For example, col. 3 (lines 15-47) discusses the use

of a production testing process that can identify defective columns and those bad column addresses are further programmed with fuses. Also, the column decoder CMDEC is the scan decoder for the testing process as the MUX counter CMCTR is advanced during testing. Fig. 1A also shows a plurality of redundant wordline drivers (COLDRVR0-COLDRVR1) acting as the claimed "redundant y-drivers" and the main decoders (XDEC, CMDEC) also acting as the claimed second circuit for testing a level of stored data in the redundant array with the help of the column MUX counter (CMCTR) as mentioned above. For example, col. 3 (lines 15-47) discusses the use of a production testing process that can identify defective columns and those bad column addresses are further programmed with fuses. Also, the column decoder CMDEC is the scan decoder for the testing process as the MUX counter CMCTR is advanced during testing. Note that cols. 4-5 mentions the use of a redundancy column comparator for comparing the column addresses that have been programmed into the fuses with the current column address to enable the redundant array if defective addresses are matched. Especially, col. 5 (lines 28-40) further mentions the compare outputs (ORs) "are used to control the two redundancy column drivers", thus obviously enable these redundant column drivers while also disable the main column drivers through the MUX column decoders (CMDEC, Fig. 1A) as well-known to one skilled in this art. Thus, from this statement, one skilled in the art can see that testing & automatic replacement for all the stored, defective data the two arrays (100, 102) is obviously performed by these two claimed "first" and "second" circuits as well.

Regarding claims **15 & 16**, Tran et al shows the use of fuses & decoders as claimed "storage circuit" for storing addresses of defective cells. See cols 5-6.

Regarding claims **17-20**, Tran et al shows the use of a 3-bit binary counter (CMCTR) as claimed "address sequencer" advancing through the addresses of failing cells/columns.

Regarding claim **27**, both plurality of main column drivers (COLDRV) and redundant column drivers (COLDRVR) are tied together and controlled by the same enable signals generated through the column MUX circuit (CMDEC).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Viet Q. Nguyen whose telephone number is (571) 272-1788. The examiner can normally be reached on 7am-6pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on (571) 272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Viet Q Nguyen
Primary Examiner
Art Unit 2827

V. Nguyen
4/11/2005